CLAIMS:

1. A field effect transistor comprising:

a pair of source/drain regions having a channel region positioned therebetween; and

a gate positioned operatively proximate the channel region, the gate comprising conductively doped semiconductive material, a silicide layer and a conductive diffusion barrier layer.

2. The transistor of claim 1 wherein the conductive diffusion barrier layer is in contact with the semiconductive material.

3. The transistor of claim 1 wherein the conductive diffusion barrier layer is not in contact with the semiconductive material.

4. The transistor of claim 1 wherein the conductive diffusion barrier layer is in contact with the silicide layer.

5. The transistor of claim 1 wherein the conductive diffusion barrier layer is in contact with both the semiconductive material and the silicide layer.

6. The transistor of claim 1 wherein the conductive diffusion barrier layer is received over the semiconductive material.

7. The transistor of claim 1 wherein the conductive diffusion barrier layer is received over the silicide layer.

8. The transistor of claim 1 wherein the conductive diffusion barrier layer is received over both the semiconductive material and the silicide layer.

9. The transistor of claim 1 wherein the silicide layer is received over the conductive diffusion barrier layer.

10. The transistor of claim 1 wherein the conductive diffusion barrier layer comprises W_xN_y.

11. The transistor of claim 1 wherein the conductive diffusion barrier layer comprises titanium.

12. The transistor of claim 11 wherein the conductive diffusion barrier layer is selected from the group consisting of TiN, TiO_xN_y, and TiW_xN_y, and mixtures thereof.

13. The transistor of claim 1 wherein the conductively doped semiconductive material comprises n+ polysilicon.

14. The transistor of claim 1 wherein the conductively doped semiconductive material comprises p+ polysilicon.

15. The transistor of claim 1 wherein the silicide layer and the conductive diffusion barrier layer comprise the same metal.

16. Integrated circuitry comprising:

a field effect transistor including a gate, a gate dielectric layer, source/drain regions and a channel region; the gate comprising semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer; and

insulative material received proximate the gate, the insulative material including semiconductive material provided therein in electrical connection with the gate, the semiconductive material provided within the insulative material being conductively doped with a conductivity enhancing impurity of a second type, the conductive diffusion barrier layer of the gate being provided between the gate semiconductive material and the semiconductive material provided within the insulative material.

17. The integrated circuitry of claim 16 wherein the first type is n and the second type is p.

18. The integrated circuitry of claim 16 wherein the first type is p and the second type is n.

19. The integrated circuitry of claim 16 wherein the gate also comprises a conductive silicide.

20. The transistor of claim 19 wherein the silicide and the conductive diffusion barrier layer comprise the same metal.

21. The integrated circuitry of claim 16 wherein the semiconductive material within the insulating material contacts the conductive diffusion barrier layer of the gate.

22. The integrated circuitry of claim 16 wherein the semiconductive material within the insulating material does not contact the conductive diffusion barrier layer of the gate.

23. The integrated circuitry of claim 16 wherein the gate also comprises a conductive silicide, the semiconductive material within the insulating material contacting the silicide.

24. The integrated circuitry of claim 16 wherein the conductive diffusion barrier layer is received over the gate semiconductive material, and the semiconductive material within the insulating material is received over the gate.

25. The integrated circuitry of claim 16 wherein the insulative material comprises an opening within which the semiconductive material therein has been provided, the opening being substantially void of any conductive diffusion barrier layer material.

26. A method of forming a field effect transistor gate comprising:

forming a layer of conductively doped semiconductive material over a substrate;

forming a layer of a conductive silicide over the substrate;

forming a conductive diffusion barrier layer over the substrate; and

removing portions of the semiconductive material layer, the silicide layer and the conductive diffusion barrier layer to form a transistor gate comprising the semiconductive material, the conductive silicide and the conductive diffusion barrier layer.

27. The transistor of claim 26 wherein the silicide layer and the conductive diffusion barrier layer comprise the same metal.

28. The method of claim 26 wherein the removing comprises:

forming a masking layer over the semiconductive material, the conductive silicide layer and the conductive diffusion barrier layer and leaving said portions unmasked by the masking layer; and

etching away the unmasked portions to form the transistor gate beneath the masking layer.

29. The method of claim 26 wherein the removing comprises:

depositing, selectively light exposing and developing a layer of photoresist to form a photoresist mask over the semiconductive material, the conductive silicide layer and the conductive diffusion barrier layer and leaving said portions unmasked by the photoresist; and

etching away the unmasked portions to form the transistor gate beneath the photoresist.

30. The method of claim 26 comprising providing the conductive diffusion barrier layer in contact with the semiconductive material layer.

31. The method of claim 26 comprising forming the conductive diffusion barrier layer after and in contact with the semiconductive material layer.

32. The method of claim 26 comprising forming the conductive diffusion barrier layer after and not in contact with the semiconductive material layer.

33. The method of claim 26 comprising providing the conductive diffusion barrier layer in contact with the silicide layer.

34. The method of claim 26 providing the conductive diffusion barrier layer in contact with both the semiconductive material layer and the silicide layer.

35. The method of claim 26 comprising forming the conductive diffusion barrier layer over the semiconductive material layer.

36. The method of claim 26 comprising forming the conductive diffusion barrier layer over the silicide layer.

37. The method of claim 26 comprising forming the conductive diffusion barrier layer over both the semiconductive material layer and the silicide layer.

38. The method of claim 26 comprising forming the silicide layer over the conductive diffusion barrier layer.

39. The method of claim 26 comprising forming the conductive diffusion barrier layer to be selected from the group consisting of TiN, TiO_xN_y, W_xN_y and TiW_xN_y, and mixtures thereof.

40. A method of forming integrated circuitry comprising:

forming a field effect transistor gate over a substrate, the gate comprising semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer;

forming an insulative layer over the substrate;

forming an opening into the insulative layer;

forming semiconductive material conductively doped with a conductivity enhancing impurity of a second type within the opening; and

providing the doped semiconductive material within the opening in electrical connection with the gate, with the conductive diffusion barrier layer of the gate being received between the semiconductive material of the gate and the semiconductive material within the opening.

41. The method of claim 40 wherein the first type is n and the second type is p.

42. The method of claim 40 wherein the first type is p and the second type is n.

43. The method of claim 40 comprising forming the gate to also comprise a conductive silicide.

44. The transistor of claim 43 wherein the silicide and the conductive diffusion barrier layer comprise the same metal.

45. The method of claim 40 comprising forming the semiconductive material within the opening to contact the conductive diffusion barrier layer of the gate.

46. The method of claim 40 wherein the semiconductive material formed within the opening does not contact the conductive diffusion barrier layer of the gate.

47. The method of claim 40 comprising forming the gate to also comprises a conductive silicide, the semiconductive material within the opening contacting the silicide.

48. The method of claim 40 wherein the opening is filled with conductive material none of which comprises any conductive diffusion barrier layer material.

49. A method of forming integrated circuitry comprising:

forming a field effect transistor gate over a substrate, the gate comprising semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer received thereover;

forming an insulative layer over the gate;

forming an opening into the insulative layer to a conductive portion of the gate; and

forming semiconductive material conductively doped with a conductivity enhancing impurity of a second type within the opening in electrical connection with the conductive portion, with the conductive diffusion barrier layer of the gate being received between the semiconductive material of the gate and the semiconductive material within the opening.

50. The method of claim 49 wherein the first type is n and the second type is p.

51. The method of claim 49 wherein the first type is p and the second type is n.

52. The method of claim 49 comprising forming the gate to also comprise a conductive silicide.

53. The method of claim 49 comprising forming the semiconductive material within the opening to contact the conductive diffusion barrier layer of the gate.

54. The method of claim 49 wherein the semiconductive material formed within the opening does not contact the conductive diffusion barrier layer of the gate.

55. The method of claim 49 comprising forming the gate to also comprises a conductive silicide, the semiconductive material within the opening contacting the silicide.

56. The method of claim 49 wherein the opening is filled with conductive material none of which comprises any conductive diffusion barrier layer material.